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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,748	09/30/2003	Nasser Nouri	33226/324001; P8928	8004
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OSHA LIANG L.L.P./SUN TWO HOUSTON CENTER 909 FANNIN, SUITE 3500 HOUSTON, TX 77010			EXAMINER LO, SUZANNE	
			ART UNIT 2128	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/675,748	Applicant(s) NOURI ET AL.	
	Examiner SUZANNE LO	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,8,11,15,18,19,22,25 and 31-42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,8,11,15,18,19,22,25 and 31-42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-5, 8, 11, 15, 18-19, 22, 25, 31-42 have been presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 34, 35, and 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 34 recites the limitation “wherein the step of executing the first simulation image on the test simulator” and it is unclear how the first simulation image is executed on the test simulator as the parent claim 11 stipulates that first simulation image is executed on the reference simulator. Claim 34 is interpreted by the Examiner to read the first simulation image executed on the reference simulator.

Claim 35 recites the limitation, “wherein the step of executing the second simulation image on the reference simulator” and it is unclear how the second simulation image is executed on the reference simulator as the parent claim 11 stipulates that the second simulation image is executed on the test reference simulator. Claim 35 is interpreted by the Examiner to read the second simulation image executed on the test simulator.

Claim 40 recites the limitation "the user data". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2128

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5, 8, 11, 15, 18-19, 22, 25, 31-32, 35, and 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over McNamara et al. (U.S. Patent No. 6,141,630) in view of Hollander (U.S. Patent No. 6,182,258 B1).

As per claim 1, McNamara is directed to a system for evaluating a simulation of a circuit design comprising: a processor; a reference simulator configured to generate golden data by executing a first simulation image using the processor, wherein the first simulation image is compiled from a first implementation of the circuit design (**column 5, lines 32-45**); a test simulator (**column 3, lines 34-37 and Figure 1, testbench 108**) configured to generate test data by executing a second simulation image, wherein the second simulation image is compiled from a second implementation of the circuit design (**column 4, line 66 – column 5, line 4**); and a comparator configured to select a portion of the test data

Art Unit: 2128

(**column 4, lines 46-57 and column 5, 38-57**), use a mapping rule of a plurality of mapping rules to identify a portion of the golden data associated with the portion of the test data, and generate a comparison result by comparing the portion of the golden data to the portion of the test data before the execution of the second simulation image on the test simulator has completed (**column 7, lines 18-36**); and wherein the comparison result is used to debug at least one selected from the group of the circuit design and the test simulator, by correcting and displaying an error detected in the comparison result (**column 7, lines 19-31**) but fails to explicitly disclose wherein the plurality of mapping rules map an internal hierarchy of the first implementation of the simulation design to an internal hierarchy of the second implementation.

Hollander teaches wherein the plurality of mapping rules map an internal hierarchy of the first implementation of the simulation design to an internal hierarchy of the second implementation (**column 12, lines 40-49**). It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of verifying a simulation design of McNamara with the mapping rules of Hollander in order to reduce the likelihood of the occurrence of a state explosion problem (**column 13, lines 38-46**).

The combination of McNamara and Hollander fails to explicitly disclose wherein *the comparison result is used to debug solely the test simulator* in a system comprising a reference simulator, test simulator and comparator. Smith teaches using a reference software (reference simulator) and test software under development (test simulator) and comparing the two to debug the test software under development (**column 2, lines 47-50, column 2, line 60 – column 3, line 10**). McNamara, Hollander, and Smith are analogous because they are all from the same field of endeavor, design verification. It would have been obvious to an ordinary person skilled in the art to combine the system of McNamara and Hollander with the method of debugging of Smith in order to identify design flaws (**column 3, lines 8-10**).

Art Unit: 2128

As per claim 2, the combination of McNamara, Hollander, and Smith already discloses the system of claim 1 further comprising: a golden data repository storing the golden data (**McNamara, column 5, lines 32-45**).

As per claim 3, the combination of McNamara, Hollander, and Smith already discloses the system of claim 1, wherein comparing the portion of the golden data to the portion of the test data occurs dynamically (**McNamara, column 7, lines 19-36**).

As per claim 4, the combination of McNamara, Hollander, and Smith already discloses the system of claim 3 further comprising: a buffer to store the golden data (**McNamara, column 5, lines 32-45**).

As per claim 5, the combination of McNamara, Hollander, and Smith already discloses the system of claim 4, wherein the comparator is configured to wait to compare the portion of the test data until after the golden data is stored in the buffer (**McNamara, column 5, lines 32-45**).

As per claim 8, the combination of McNamara, Hollander, and Smith already discloses the system of claim 1, wherein the mapping rule is obtained while the test simulator is halted (**Hollander, column 12, lines 40-49**).

As per claim 11, McNamara is directed to a method of evaluating a simulation of a circuit design comprising: executing a first simulation image on a reference simulator to obtain golden data, wherein the first simulation image is obtained by compiling a first implementation of the circuit design (**column 5, lines 32-45**); executing a second simulation image on a test simulator to obtain test data, wherein the second simulation image is obtained by compiling a second implementation of the circuit design (**column 3, lines 34-37 and Figure 1, testbench 108**) to obtain test data (**column 4, line 66 – column 5, line 4**); selecting a portion of the test data (**column 4, lines 46-57 and column 5, 38-57**); using a mapping rule of a plurality of mapping rules to identify a portion of the golden data associated with the portion of the test data (**column 7, lines 18-36**); and comparing the portion of the golden data to the portion of the test data

Art Unit: 2128

to obtain a comparison result (**column 7, lines 18-36**) wherein the comparison result is used to debug at least one selected from the group of the simulation design and the test simulator, by correcting and displaying an error detected in the comparison result (**column 7, lines 19-31**) but fails to explicitly disclose wherein the plurality of mapping rules map an internal hierarchy of the first implementation of the simulation design to an internal hierarchy of the second implementation.

Hollander teaches wherein the plurality of mapping rules map an internal hierarchy of the first implementation of the simulation design to an internal hierarchy of the second implementation (**column 12, lines 40-49**). It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of verifying a simulation design of McNamara with the mapping rules of Hollander in order to reduce the likelihood of the occurrence of a state explosion problem (**column 13, lines 38-46**).

The combination of McNamara and Hollander fails to explicitly disclose wherein *the comparison result is used to debug solely the test simulator* in a system comprising a reference simulator, test simulator and comparator. Smith teaches using a reference software (reference simulator) and test software under development (test simulator) and comparing the two to debug the test software under development (**column 2, lines 47-50, column 2, line 60 – column 3, line 10**). McNamara, Hollander, and Smith are analogous because they are all from the same field of endeavor, design verification. It would have been obvious to an ordinary person skilled in the art to combine the system of McNamara and Hollander with the method of debugging of Smith in order to identify design flaws (**column 3, lines 8-10**).

As per claim 15, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11 further comprising: storing the golden data in a golden data repository (**McNamara, column 5, lines 32-45**).

Art Unit: 2128

As per claim 18, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11, wherein the step of comparing the selected golden data to the selected test data waits on storing the golden data in a buffer (**McNamara, column 5, lines 32-45**).

As per claim 19, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11, wherein the step of selecting a portion of the test data is performed dynamically (**McNamara, column 4, lines 46-57**).

As per claim 22, the combination of McNamara, Hollander, and Smith already discloses the method of claim 21, wherein the step of executing the simulation image is halted to obtain the user data (**McNamara, column 4, lines 46-57**).

As per claims 25 and 37-39, McNamara is directed to a computer system for evaluating a simulation design comprising: a processor; a memory; a storage device; and software instructions (**column 6, lines 20-31**) stored in the memory for enabling the computer system to perform method steps with the same limitations as claims 11, and 31-32, and is therefore rejected over the same prior art combination.

As per claim 31, the combination of McNamara, Hollander, and Smith already discloses the system of claim 1, wherein the test simulator executes the second simulation image in lockstep *with execution of the first simulation image* (**Hollander, column 12, lines 40-48**).

As per claim 32, the combination of McNamara, Hollander, and Smith already discloses the system of claim 1, wherein the reference simulator executes the first simulation image in lockstep *with execution of the second simulation image* (**Hollander, column 12, lines 40-48**).

As per claim 34, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11, wherein the step of executing the first simulation image on the test simulator *is performed in lockstep with the step of executing the second simulation image* (**Hollander, column 12, lines 40-48**).

Art Unit: 2128

As per claim 35, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11, wherein the step of executing the second simulation image on the reference simulator *is performed in lockstep with the step of executing the first simulation image* (**Hollander, column 12, lines 40-48**).

As per claim 40, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11, wherein the user data is altered while executing the second simulation image (**Smith, column 4, lines 28-31**).

As per claim 41, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11, wherein the test simulator is debugged while executing the second simulation image (**Smith, Figure 6**).

As per claim 42, the combination of McNamara, Hollander, and Smith already discloses the method of claim 11, wherein the comparison result is displayed while executing the second simulation image (**Hollander, Figure 7**).

4. Claims 33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over McNamara et al. (U.S. Patent No. 6,141,630) in view of Hollander (U.S. Patent No. 6,182,258 B1) in further view of **Gupte et al. (U.S. Patent No. 5,812,416)**.

As per claim 33, the combination of McNamara and Hollander already discloses the system of claim 1 but fails to explicitly disclose wherein the portion of the test data is generated after the golden data is generated. Gupte teaches generating golden data before generating test data (**Figure 5, column 6, lines 52-63**). McNamara, Hollander, and Gupte are analogous art because they are all from the same field of endeavor, evaluating a simulation of a circuit design. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the system of evaluating a simulation of

Art Unit: 2128

McNamara and Hollander with the generation order of golden and test data of Gupte in order to allow the operation of an ASIC to be verified during various states of synthesis (**Gupte, column 2, lines 15-20**).

As per claim 36, the combination of McNamara and Hollander already discloses the method of claim 11 but fails to explicitly disclose wherein the portion of the test data is generated after the golden data is generated. Gupte teaches generating golden data before generating test data (**Figure 5, column 6, lines 52-63**). McNamara, Hollander, and Gupte are analogous art because they are all from the same field of endeavor, evaluating a simulation of a circuit design. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the system of evaluating a simulation of McNamara and Hollander with the generation order of golden and test data of Gupte in order to allow the operation of an ASIC to be verified during various states of synthesis (**Gupte, column 2, lines 15-20**).

Response to Arguments

5. Applicant's arguments filed 08/15/08 have been fully considered but they are not persuasive.
6. The 35 U.S.C. 101 rejection is withdrawn due to the amended claims.
7. The 35 U.S.C. 112 rejection of claims 31-32, and 37-38 has been withdrawn due to the amended claims. However, the 112 rejection of claims 34-35 are maintained as the claims have not been amended and the issues have not been resolved. See Section 2 above.
8. In regards to the 103 rejection of the prior art, Applicant correctly assumed that the claims stand rejected as being unpatentable over McNamara in view of Hollander. Applicant's arguments with respect to the prior art rejection have been considered but are moot in view of the new grounds of rejection.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 6,678,645 B1 issued to Rajsuman et al. on 01/13/04.
2. U.S. Patent No. 6,625,759 B1 issued to Petsinger et al. on 09/23/03.
3. U.S. Patent No. 7,139,936 B2 issued to Petsinger et al. on 11/21/06.
4. U.S. Patent No. 6,606,721 B1 issued to Gowin, Jr. et al. on 08/12/03.
5. U.S. Patent No. 5,928,334 issued to Mandyam et al. on 07/27/99.
6. U.S. Patent No. 5,920,490 issued to Peters on 07/06/99.
7. U.S. Patent Application Publication 2005/0120278 A1 published by Smith et al. on 06/02/05.
8. U.S. Patent No. 7,017,150 B2 issued to Lam et al. on 03/21/06.

10. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

Art Unit: 2128

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit
2128

SL
12/19/08